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Description

Resistor Tuning

Background of Invention

[0001] *1. Technical Field*

[0002] The present invention relates to methods for tuning (i.e., trimming) resistors of a chip, and more particularly, to a method for tuning resistors of a chip that can be used both before and after chip packaging.

[0003] *2. Related Art*

[0004] Conventional manufacturing controls on processes for forming passive devices, such as resistors in CMOS (Complementary Metal Oxide Silicon) chips, fall short of current circuit design requirements. Current industry standard I/O (Input/Output) specifications are exceeding what can be achieved in current manufacturing processes. Within analog and RF (radio frequency) semiconductors, the need for tuning the electrical resistance values of the resistors on an integrated circuit to a specific nominal value is growing to meet complex design specification re-

quirements. Manufacturing excess chips and then sorting for required parameters is one solution, but this is a costly and not consistent with manufacturing techniques. Laser ablation is used to trim in the manufacture of some precision passive devices, but this process is inconsistent with the CMOS/BiCMOS or Analog process flow as a measurement and feedback loop is required as well as individual laser trimming of a multitude of devices on a single chip. A third known solution is to design active controls into the circuitry to compensate for manufacturing variability, but this takes up space, increases complexity, and can lead to trade-offs in performance.

[0005] Therefore, there is a need for a novel resistance structure that can be tuned to a specification. Also, there is a need for a method for tuning the novel resistance structure.

SUMMARY OF INVENTION

[0006] The present invention provides a resistor structure, comprising (a) an electrically conducting region; (b) a liner region coupled to the electrically conducting region; and (c) first and second contact regions electrically coupled to the electrically conducting region and the liner region, wherein in response to a current flowing in the electrically conducting region and from the first contact region to the

second contact region, a void region in the electrically conducting region expands due to electromigration so as to increase the resistance of the resistor structure between the first and second contact regions.

[0007] The present invention also provides a method for tuning a resistor structure, the method comprising the steps of (a) providing (i) an electrically conducting region, (ii) a liner region coupled to the electrically conducting region, and (iii) first and second contact regions electrically coupled to the electrically conducting region and a liner region; and (b) flowing a current in the electrically conducting region and from the first contact region to the second contact region such that a void region in the electrically conducting region expands due to electromigration so as to increase the resistance of the resistor structure between the first and second contact regions.

[0008] The present invention also provides a providing in the resistor structure (i) a semiconductor region, (ii) an electrically conducting layer formed on the semiconductor region, (iii) a plurality of contact regions electrically coupled to the electrically conducting layer; (b) selecting first and second contact regions of the plurality of contact regions such that if intervals of the electrically conducting layer

between the first and second contact regions are replaced by a void region due to electromigration, the resistance of the resistor structure between third and fourth contact regions of the plurality of contact regions is within a predetermined tolerance of a pre-specified target resistance value; and (c) applying a voltage difference between the first and second contact regions until the intervals of the electrically conducting layer between the first and second contact regions are replaced by the void region due to electromigration.

BRIEF DESCRIPTION OF DRAWINGS

[0009] FIG. 1A illustrates a cross-sectional view of a resistor structure, in accordance with embodiments of the present invention.

[0010] FIG. 1B illustrates a view along a line 1B-1B of the resistor structure of FIG. 1A.

[0011] FIG. 1C illustrates the resistor structure of FIG. 1A after tuning, in accordance with embodiments of the present invention.

[0012] FIG. 1D illustrates the relationship between the resistance and tuning time of the resistor structure of FIG. 1A, in accordance with embodiments of the present invention.

[0013] FIG. 2A illustrates a top view of another resistor structure,

in accordance with embodiments of the present invention.

[0014] FIGs. 2Bi and 2Bii illustrate two views along lines 2Bi-2Bi and 2Bii-2Bii, respectively, of the resistor structure of FIG. 2A.

[0015] FIG. 2C illustrates the resistor structure of FIG. 2A after tuning, in accordance with embodiments of the present invention.

[0016] FIG. 3A illustrates a cross-sectional view of yet another resistor structure, in accordance with embodiments of the present invention.

[0017] FIG. 3B illustrates a view along a line 3B-3B of the resistor structure of FIG. 3A.

[0018] FIG. 3C illustrates the resistor structure of FIG. 3A after tuning, in accordance with embodiments of the present invention.

[0019] FIG. 4A illustrates a top view of yet another resistor structure, in accordance with embodiments of the present invention.

[0020] FIG. 4B illustrates a view along a line 4B-4B of the resistor structure of FIG. 4A.

[0021] FIG. 4C illustrates the resistor structure of FIG. 4A after tuning, in accordance with embodiments of the present invention.

[0022] FIGs. 5A1 and 5A2 illustrate cross-sectional views of yet another resistor structure before and after tuning, respectively, in accordance with embodiments of the present invention.

[0023] FIGs. 5B1 and 5B2 illustrate cross-sectional views of yet another resistor structure before and after tuning, respectively, in accordance with embodiments of the present invention.

[0024] FIG. 6 illustrates a flow chart of a method for tuning resistors, in accordance with embodiments of the present invention.

DETAILED DESCRIPTION

[0025] FIG. 1A illustrates a cross-sectional view of a resistor structure 100, in accordance with embodiments of the present invention. Illustratively, the resistor structure 100 comprises a copper wire 110 surrounded by an electrically conducting liner layer 120. The two ends (hereafter, referred to as the first and second ends) of the copper wire 110 are electrically coupled to the vias 130a and 130b, respectively. In one embodiment, the first end of the copper wire 110 is electrically coupled to the via 130a through the electrically conducting liner layer 120, and the second end of the copper wire 110 is in direct physical

contact with the via 130b.

[0026] FIG. 1B illustrates a view along line 1B-1B of the resistor structure 100 of FIG. 1A, in accordance with embodiments of the present invention. FIG. 1B shows that the copper wire 110 is surrounded by the liner layer 120. In an alternative embodiment, the resistor structure 100 could have the conducting liner layer 120 incorporated only on the side walls and below the wire 110 and a non-conducting passivation layer formed on the top surface on the wire 110. This would be consistent with standard BEOL damascene Cu processing techniques that do not use electrolysis plating to form a conducting liner atop surfaces of exposed wires 110.

[0027] FIG. 1C illustrates the resistor structure 100 of FIG. 1A after tuning, in accordance with embodiments of the present invention. In one embodiment, a voltage difference is applied between the vias 130a and 130b with the via 130b having a higher voltage than the via 130a. As a result, a current flow through the resistor structure 100 from the via 130b to the via 130a. In essence, the current comprises electrons flowing from the via 130a to the via 130b. The magnitude of the current is calculated such that electromigration occurs in the copper wire 110, but

not in the liner layer 120. Electromigration is a phenomenon in which atoms of a conductor, under the effect of a current flowing in the conductor, migrate in the conductor in the direction of the flow of the charged particles of the current. Here, the charged particles are electrons flowing from the via 130a to the via 130b. As a result, copper atoms of the copper wire 110 migrate in the direction of the flow of the electrons in the copper wire 110 (i.e., direction 128). As a result of electromigration occurring in the copper wire 110, a void region (empty space) 140 forms and grows in the copper wire 110, from the contact surface 140a between the liner layer 120 and the copper wire 110, and in the direction of the flow of the electrons (i.e., the direction 128). Because the resistor structure 100 loses a good conducting portion to the void region 140, the electrical resistance of the resistor structure 100 between the vias 130a and 130b is increased.

[0028] FIG. 1D illustrates the relationship between the electrical resistance R of the resistor structure 100 of FIG. 1A between the vias 130a and 130b and tuning time t during which a flow of electrons sufficiently strong to cause electromigration to occur in the copper wire 110, but not in the liner layer 120, flows through the resistor structure

100, in accordance with embodiments of the present invention. With reference to FIGs. 1A, 1B, 1C, and 1D, initially (i.e., $t = 0$), $R = R_0$, which is an initial resistance value. Then, for $t > 0$, the void region 140 (FIG. 1C) starts growing from the contact surface 140a, but has not spread vertically across the width of the wire 110 (i.e., in and opposite to the direction 129 of FIG. 1C). As a result, R is almost unchanged. At time $t = t_{void}$, the void region 140 extends across the width of the wire 110, and as a result, R jumps to value R_v, which is determined by the resistance of the liner section 120a (FIG. 1C) of the resistor structure 100 (the resistance of the remaining section 120b of the resistor structure 100 is small and negligible compared with the resistance of the liner section 120a). After that (i.e., $t > t_{void}$), R increases at a constant rate which depends on the speed of growth of the void region 140 in the direction of the flow of electrons (i.e., the direction 128). Finally, at $t = t_f$, the tuning of the resistor structure 100 is complete and the applied voltage is removed because $R = R_{target}$, which is the target value of R. At this time, the void region 140 grows to a surface 140b between the void region 140 and the copper wire 110.

[0029] FIG. 2A illustrates a top view of a resistor structure 200, in

accordance with embodiments of the present invention. Illustratively, the resistor structure 200 comprises a copper wire 210 surrounded by an electrically conducting liner layer 220. One end (hereafter, referred to as the first end) of the copper wire 210 is electrically coupled to the via 230a and the other end (hereafter, referred to as the second end) of the copper wire 210 is electrically coupled to, illustratively, the vias 230b1 and 230b2. In one embodiment, the first end of the copper wire 210 is electrically coupled to the via 230a through the electrically conducting liner layer 220, and the second end of the copper wire 210 is in direct physical contact with the vias 230b1 and 230b2. The resistor structure 200 comprises two sections 250a and 250b. The section 250a has the same structure as the section 250b, but has a smaller width.

[0030] FIGs. 2Bi and 2Bii illustrate two views along lines 2Bi-2Bi and 2Bii-2Bii, respectively, of the resistor structure of FIG. 2A. As shown in FIGs. 2Bi and 2Bii, in both the sections 250a and 250b of the resistor structure 200, the copper wire 210 is at the center of the resistor structure 200 surrounded by the electrically conducting liner layer 220. The liner layer 220 comprises a material less electrically conducting than the material of the wire 210 (i.e., copper).

Similar to the earlier structure 100, this resistor structure 200 could also have the conducting liner layer 220 integrated only on the side walls and below the wire 210 and a non-conducting passivation layer formed on the top surface on the wire 210.

[0031] FIG. 2C illustrates the resistor structure 200 of FIG. 2A after tuning, in accordance with embodiments of the present invention. In one embodiment, a voltage difference is applied between the first and second ends of the copper wire 210. More specifically, the higher voltage potential of the voltage difference is applied to both the vias 230b1 and 230b2 and the lower voltage potential of the voltage difference is applied to the via 230a. As a result, a current flow through the resistor structure 200 from the via 230a to the vias 230b1 and 230b2 (i.e., the direction 228). The magnitude of the current is calculated such that electromigration occurs for the copper wire 210 in the section 250a, but not in the section 250b. This is because electromigration occurs only where the current density exceeds a minimum value. Therefore, if the magnitude of the current flowing through the resistor structure 200 is such that the current density in the section 250a exceeds the minimum value and current density in the section

250b does not exceed the minimum value, then electromigration occurs for the copper wire 210 in the section 250a, but not in the section 250b.

[0032] As a result of electromigration occurring in only the section 250a of the copper wire 210, a void region (empty space) 240 forms and grows in the copper wire 210 from the contact surface 240a between the liner layer 220 and the copper wire 210, and in the direction of the flow of the electrons constituting the current (i.e., the direction 228). The void region 240 grows but stops at the interface surface 240b between the section 250a and section 250b. Because the resistor structure 200 loses a good conducting portion to the void region 240, the resistance of the resistor structure 200 between the first end (vias 230a) and the second end (vias 230b1 and/or 230b2) of the resistor structure 200 is increased.

[0033] The resistor structure 200 allows for more resistance tuning control. Because electromigration is restricted to the section 250a of the resistor structure 200, the resistance of the resistor structure 200 cannot exceed a maximum value regardless of tuning duration.

[0034] FIG. 3A illustrates a cross-sectional view of a resistor structure 300, in accordance with embodiments of the

present invention. Illustratively, the resistor structure 300 comprises a copper plate 310 sandwiched between two plates 320a and 320b made of TaN (tantalum nitride), which is a material less electrically conducting than copper. In general, the two plates 320a and 320b can comprise any material less electrically conducting than copper such as TiN, NiCr and SiCr. The two ends of the plate 320a are in direct physical contact with the two vias 330a and 330b.

[0035] FIG. 3B illustrates a view along the line 3B-3B of the resistor structure 300 of FIG. 3A. As shown in FIG. 3B, the copper plate 310 is sandwiched between the two TaN plates 320a and 320b.

[0036] FIG. 3C illustrates the resistor structure 300 of FIG. 3A after tuning, in accordance with embodiments of the present invention. In one embodiment, a voltage difference is applied between the vias 330a and 330b with the via 330b having a higher voltage than the via 330a. As a result, a current flow through the resistor structure 300 from the via 330b to the via 330a. In essence, the current comprises electrons flowing from the via 330a to the via 330b. The magnitude of the current is calculated such that electromigration occurs in the copper plate 310, but

not in the two TaN plates 320a and 320b. As a result, a void region 340 forms and grows in the copper plate 310, from the end surface 340a of the copper plate 310, and in the direction of the flow of electrons (i.e., the direction 328). Because the resistor structure 300 loses a good conducting portion to the void region 340, the resistance of the resistor structure 300 between the vias 330a and 330b is increased. In this structure 300, the resistance increase when the void region 340 extends completely across the wire 310 would be 100-1000%, and, as a result of this substantial resistance increase rate, the time required to tune the resistance during electromigration stressing would be reduced.

[0037] FIG. 4A illustrates a top view of a resistor structure 400, in accordance with embodiments of the present invention. Illustratively, the resistor structure 400 comprises a silicide layer 410 formed on a Si layer 440 (FIG. 4B) or any type of materials that will react to form a metallic composite layer. A first end of the silicide layer 410 is electrically coupled to interconnect region 420a1 through the via 430a1 and to interconnect region 420a2 via the vias 430a2 and 430a3. A second end of the silicide layer 410 is electrically coupled to interconnect region 420b1

through the via 430b1 and to interconnect region 420b2 through the vias 430b2 and 430b3.

[0038] FIG. 4B illustrates a view along a line 4B-4B of the resistor structure 400 of FIG. 4A. Shown from top down are the silicide layer 420 and the Si layer 440.

[0039] FIG. 4C illustrates the resistor structure 400 of FIG. 4A after tuning, in accordance with embodiments of the present invention. In one embodiment, a voltage difference is applied between the vias 430a1 and 430b1 (through the interconnect regions 420a1 and 420b1, respectively) with the via 430b1 having a higher voltage than the via 430a1. The voltage difference is such that electromigration occurs in the silicide plate 410. Optimizing the design in order to induce current crowding, current densities in the silicide plate 410 are larger at points closer to an imaginary straight line connecting the vias 430a1 and 430b1. As a result, it is feasible to cause electromigration to occur only in a portion 410a of the silicide plate 410 near the imaginary straight line connecting the vias 430a1 and 430b1. In one embodiment, electromigration in the portion 410a is maintained for a period of time long enough so that the silicide material in the portion 410a of the silicide plate 410 disappears and what is left

is a nonsilicide Si region 450. Because the resistor structure 400 loses the good conducting material (silicide) in the portion 410a, the resistance of the resistor structure 400 between the interconnect regions 420a2 and 420b2 is increased.

[0040] FIG. 5A1 illustrates a cross-sectional view of a resistor structure 500, in accordance with embodiments of the present invention. Illustratively, the resistor structure 500 comprises a silicide layer 510 formed on silicon region 520. The resistor structure 500 further comprises, illustratively, vias 530.1, 530.2, 530.3, 530.4, 530.5, 530.6, and 530.7 being spread along and in electrical contact with the silicide layer 510. In one embodiment, the vias 530.1, 530.2, 530.3, 530.4, 530.5, 530.6, and 530.7 are evenly spread along the silicide layer 510.

[0041] FIG. 5A2 illustrates the resistor structure 500 of FIG. 5A1 after tuning, in accordance with embodiments of the present invention. In one embodiment, a voltage difference is applied between the vias 530.2 and 530.4 with the via 530.4 having a higher voltage than the via 530.2. As a result, a current flows through the silicide layer 510 from the via 530.4 to the via 530.2. In essence, the current comprises electrons flowing in the silicide layer 510 from

the via 530.2 to the via 530.4. The voltage difference and the sizes and shapes of the silicide layer 510 are such that electromigration occurs only in the silicide layer 510. As a result of electromigration occurring in the silicide layer 510, a nonsilicide Si region 540 with no silicide forms and grows in the silicide layer 510 from a point 540a under the via 530.2, and in the direction of the flow of the electrons constituting the current (i.e., the direction 528). In one embodiment, the tuning time is long enough such that the nonsilicide Si region 540 extends to a point 540b under the via 530.4. Because the resistor structure 500 loses a good conducting portion to the nonsilicide Si region 540, the resistance of the resistor structure 500 between the vias 530.1 and 530.7 is increased.

[0042] In the embodiment described above, two intervals of the silicide layer 510 are replaced by the nonsilicide Si region 540. The first interval is between the via 530.2 and via 530.3. The second interval is between the via 530.3 and via 530.4. In an alternative embodiment, the tuning of the resistor structure 500 described above can be performed in two steps. The first step involves applying a voltage difference between the vias 530.2 and 530.3 with the via 530.3 having a higher voltage than the via 530.2 so as to

expand the nonsilicide Si region 540 throughout the first interval of the silicide layer 510. The second step involves applying a voltage difference between the vias 530.3 and 530.4 with the via 530.4 having a higher voltage than the via 530.3 so as to expand the nonsilicide Si region 540 throughout the second interval of the silicide layer 510.

[0043] In general, given a pre-specified target resistance value for the resistor structure 500 (FIG. 5A1) between the vias 530.1 and 530.7, it can be calculated how many intervals of the silicide layer 510 should be replaced by the nonsilicide Si region 540 so that the resulting resistor structure 500 has a resistance value within a pre-determined tolerance of the pre-specified target resistance value. For example, suppose that after calculation, three intervals of the silicide layer 510 should be replaced by the nonsilicide Si region 540. As a result, a voltage difference can be applied between the via 530.2 and the via 530.5 of the resistor structure 500 (FIG. 5A1). The magnitude and duration of the applied voltage difference are such that the nonsilicide Si region 540 expands in the silicide layer 510 all the way from the via 530.2 to the via 530.5.

[0044] FIGs. 5B1 and 5B2 illustrate cross-sectional views of yet another resistor structure 550 before and after tuning, re-

spectively, in accordance with embodiments of the present invention. With reference to FIG. 5B1, the resistor structure 550 comprises illustratively a Si region 560, a dielectric layer 590 formed on the Si region 560, a silicide layer 570 which comprises two separate sections 570a and 570b. The dielectric layer 590 is used as a mask in the formation of the silicide layer sections 570a and 570b. The resistor structure 550 further comprises vias 580.1, 580.2, 580.3, and 580.4 electrically coupled to the silicide layer 570.

[0045] FIG. 5B2 illustrates the resistor structure 550 after tuning. More specifically, tuning can be performed by applying a voltage difference to the vias 580.2 and 580.3 with the via 580.2 being at a lower voltage than the via 530.3 such that electromigration occurs in the silicide layer section 570b. As a result, the non-silicide Si region 595 extends to the right (i.e., direction 597) in the direction of the flow of the electrons. Because the resistor structure 550 loses a good conducting region to the non-silicide Si region 595, the resistance of the resistor structure 550 between the vias 580.1 and 580.4 is increased.

[0046] The resistance of the resistor structure 550 between the vias 580.1 and 580.4 before tuning (FIG. 5B1) is deter-

mined essentially by the resistive Si region 598 beneath the dielectric layer 590. After tuning, this resistive Si region 598 extends further in the direction 597 to the via 580.3 (i.e., to include the non-silicide Si region 595). As a result, the length of the non-silicide Si region 595 compared with the length of the Si region beneath the dielectric layer 590 determines the resistance increase percentage of the resistor structure 550. For example, if the non-silicide Si region 595 is half the length of the dielectric layer 590, the resistance increase percentage of the resistor structure 550 is 50%. As a result of this gradual resistance increase rate, this structure resistor 550 would allow one to implement very fine tuning of the resistance required for the most precise circuit requirements.

[0047] On the contrary, the resistance of the resistor structure 500 (FIG. 5A1) between the vias 530.1 and 530.7 before tuning is determined essentially by the silicide layer 510 which has a relatively low resistance (because silicide is a good conducting material). However, the resistance of the resistor structure 500 between the vias 530.1 and 530.7 after tuning (FIG. 5A2) is determined essentially by the non-silicide Si region 540 which has a relatively high resistance (because Si is not a good conducting material

compared with silicide). Therefore, the resistance increase is substantial. As a result of this substantial resistance increase rate, this structure 500 would allow one to reduce tuning time, which is important in the case where a large number of resistors are to be tuned.

[0048] FIG. 6 illustrates a flow chart of a method 600 for tuning multiple resistors, one at a time, in accordance with embodiments of the present invention. The multiple resistors to be tuned can be similar to the resistor structures 100, 200, 300, 400, and 500 (FIGs. 1A, 2A, 3A, 4A, and 5A, respectively). For illustration, assume that multiple resistors 100 are to be tuned using the method 600. The method 600 starts at step 610 in which the resistance of a first (or next) resistor 100 is measured. In one embodiment, the resistor"s resistance can be measured by applying a voltage difference across the resistor 100 and measuring the resulting current flowing through the resistor 100. Then, in step 620, a determination is made as to whether the measured resistance at least equals a pre-specified target resistance value. If no, in step 630, the resistor is tuned (i.e., its resistance is increased) until its resistance at least equals the target resistance value. More specifically, in one embodiment, a voltage difference can be applied

across the resistor 100 between the vias 130a and 130b. The voltage difference is such that electromigration occurs only in the copper wire 110, but not in the liner layer 120. At the same time, the resulting current is measured. As a result, the resistance of the resistor 100 can be computed at any time (i.e., resistance monitoring). When the resistance of the resistor 100 exceeds the pre-specified target resistance value, the applied voltage difference is removed from the resistor 100. In an alternative embodiment, the applied voltage difference is removed from the resistor 100 as soon as the resistance of the resistor 100 between the vias 130a and 130b is within a pre-determined tolerance of the pre-specified target resistance value. After step 630, the method 600 goes to step 640.

[0049] If the answer to the question in step 620 is affirmative, the method 600 skips to step 640. In step 640, a determination is made as to whether the resistor 100 is the last one to be tuned. If yes, the method 600 stops. If the answer to the question in step 640 is negative, the method 600 loops back to step 610 where the resistance of the next resistor 100 to be tuned is measured.

[0050] In summary, a resistor structure according to embodi-

ments of the present invention comprises an electrically conducting region coupled to a liner region. Both the electrically conducting region and the liner region are electrically coupled to first and second contact regions. A voltage difference is applied between the first and second contact regions. As a result, a current flows between the first and second contact regions in the electrically conducting region. The voltage difference and the materials of the electrically conducting region and the liner region are such that electromigration occurs only in the electrically conducting (very low resistive) region. As a result, a void region expands in the electrically conducting region in the direction of the flow of the charged particles constituting the current. Because the resistor structure loses a conducting portion of the electrically conducting region to the void region, the resistance of the resistor structure is increased (i.e., tuned). In general, the void region is not necessarily vacuum. Here, the void region comprises what is left after some electrically conducting materials of the electrically conducting region has migrated away due to electromigration. For instance, the nonsilicide Si region 540 (FIG. 5A2) can be called a void region, comprising what is left after silicide has migrated away.

[0051] In the embodiments described above, copper and silicide materials are used. In general, any material in which electromigration occurs in response to sufficiently strong current can be used.

[0052] While particular embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.